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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of			
Edwin C. Kan et al.			Group Art Unit No. 2818
Application No.	:	10/718,662	Examiner:
Filed	:	November 24, 2003	
For	:	Multibit Metal Nanocrystal Memories and Fabrication	

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the provisions of 37 CFR 1.97 and 1.98, applicants hereby submit the documents listed on the attached PTO-1449B.

Copies of the cited publications are enclosed. Copies of the cited patents have not been included, but will be furnished upon request.

Respectfully submitted,

Edwin C. Kan et al.
Applicant

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August 13, 2004

PTO/SB/08b(05-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 3

Complete if Known	
Application Number	10/718,662
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First Named Inventor	Edwin C. Kan
Art Unit	2818
Examiner Name	
Attorney Docket Number	CRF D-2768D/Kan

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	"The Evolution of Dram Cell Technology," B. El-Kareh, G.B. Bronner; Solid State Technology, May 1997, Vol. 40, Issue 5	
	2	"Fast and Long Retention-Time Nano-Crystal Memory," H.I. Hanafi, S. Tiwari, I. Khan; IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996	
	3	"Charge-Trap Memory Device Fabricated by Oxidation of $Si_{1-x}Ge_x$," Y-C King, T-J King, C. Hu; IEEE Transactions on Electron Devices, Vol. 48, No. 4, April 2001	
	4	"A Long-Refresh Dynamic/Quasi-Nonvolatile Memory Device with 2-nm Tunneling Oxide," Y-C King, T-J King, C. Hu; IEEE Electron Device Letters, Vol. 20, No. 8, August 1999	
	5	"NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, D. Finzi; IEEE Electron Device Letters, Vol. 21, No. 11, November 2000	
	6	"A Low Voltage SONOS Nonvolatile Semiconductor Memory Technology," M.H. White, Y. Yang, A. Purwar, M.L. French; IEEE Transactions on Components, Packaging, and Manuf. Tech.-Part A, Vol. 20, No. 2, June 1997	
	7	"High-Endurance Ultra-Thin Tunnel Oxide in MONOS Device Structure for Dynamic Memory Application," H.C. Wann, C. Hu; IEEE Electron Device Letters, Vol. 16, No. 11, November 1995	
	8	"Programming Characteristics of P-Channel Si Nano-Crystal Memory," K. Han, I. Kim, H. Shin; IEEE Electron Device Letters, Vol. 21, No. 6, June 2000	
	9	"A Novel, aerosol-nanocrystal floating-gate device for non-volatile memory applications," J. DeBlauwe, M. Ostraat, M.L. Green, G. Weber, T. Sorsch, A Kerber, F. Klemens, et al.; 2000 IEEE	

Examiner Signature		Date Considered	

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	10	"Single-Electron Devices and Their Applications," K.K. Likharev; Proceedings of the IEEE, Vol. 87, No. 4, April 1999	
	11	"Non-Volatile Si Quantum Memory with Self-Aligned Doubly-Stacked Dots," R. Ohba, N. Sugiyama, K. Uchida, J. Koga, A. Toriumi; IEEE 2000	
	12	"Modification of Indium Tin Oxide for Improved Hole Injection in Organic Light Emitting Diodes," Y. Shen, D.B. Jacobs, G.G. Malliaras, G. Koley, M.G. Spencer, A. Ioannidis; Adv. Mater. 2001, No. 16, 8/16	
	13	"Room Temperature Operation of a Quantum-Dot Flash Memory," J.J. Welser, S. Tiwari, S. Rishton, K.Y. Lee, Y. Lee; IEEE Electron Device Letters, Vol. 18, No. 6, June 1997	
	14	"Silicon Nano-Crystals Based MOS Memory and Effects of Traps on Charge Storage Characteristics," Y. Shi, S.L. Bu, X.L. Yuan,Y.D. Zheng; K. Saito, H. Ishikuro, T. Hiramoto; IEEE 1998	
	15	"A High Capacitive-Coupling Ratio (HiCR) Cell for 3 V-Only 64 Mbit and Future Flash Memories,"Y.S. Hisamune, K. Kanamori, T. Kubota, Y. Suzuki, M. Tsukiji, E. Hasegawa, A. Ishitani, T. Okazawa, IEEE 1993	
	16	"Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage," S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, D. Buchanan; 1995 IEEE	
	17	"Multilevel FLash cells and their Trade-offs," B. Eitan, R. Kazer-ounian, A. Roy; G. Crisenza, P. Cappelletti, A. Modelli; 1996 IEEE	
	18	"Modeling and Design Study of Nanocrystal Memory Devices," M. She, Y-C King, T-J King, C. Hu; Dept. of Elect. Eng. and Comp. Sciences, U. of C., Berkely, CA	
	19	"A Four-State EEPROM Using Floating-Gate Memory Cells," C. Bleiker, H. Melchior; IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, June 1987	

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	20	"A Multilevel Approach Toward Quadrupling the Density of Flash Memory," D.L. Kencke, R. Richart, S. Garg, S.K. Banerjee; IEEE Electron Device Letters, Vol. 19, No. 3, March 1998	
	21	"Data Retention of a SONOS Type-Two-Bit Storage Flash Memory Cell," W.J. Tsai, N.K. Zous, C.J. Liu, C.C. Liu, C.H. Chen, T. Wang, S. Pan, C-Y Lu; S.H. Gu; 2001 IEEE	
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	23	"On the Universality of Inversion Layer Mobility in Si MOSFET's: Part I-Effects of Substrate Impurity Concentration," S-i Takagi, A. Toriumi, M. Iwase, H. Tango; IEEE Transactions on Electron Devices, Vol. 41, No. 12, December 1994	
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